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1. A fabrication method for heterojunction bipolar transistor, said method comprising:

providing a substrate having a collector therein, a base layer over said substrate, an oxide layer over said base layer, and a polysilicon layer over said oxide layer;

forming a first photoresist layer over said polysilicon layer;

transferring a line pattern into said first photoresist layer by a photo mask with said line pattern to form a emitter window pattern;

etching said polysilicon layer to expose said oxide layer by using said emitter window pattern as an etching mask;

performing a first ion implantation process into said base layer to form a first extrinsic base region therein;

removing said emitter window pattern;

forming a dielectric layer over said polysilicon layer and said oxide layer;

thinning said dielectric layer to expose said polysilicon layer;

removing said polysilicon layer to expose said oxide layer;

etching said exposed oxide layer to expose said base layer;

forming an emitter layer over said base layer and said dielectric layer;

forming a second photoresist layer over said emitter layer;

transferring an emitter pattern into said second photoresist layer;

etching said emitter layer to form an emitter and expose said oxide layer by using said emitter pattern as an etching mask; and

performing a second ion implantation process to form a second extrinsic base region.

2. The method according to claim 1, wherein said oxide layer comprises an in situ steam generation oxide layer.

3. The method according to claim 1, further comprising a step of forming a bottom anti-reflecting coating layer over said polysilicon layer.

4. The method according to claim 1, wherein said polysilicon layer comprises an undoped polysilicon layer.

5. The method according to claim 1, wherein said dielectric layer comprises a SiN layer.

6. The method according to claim 1, wherein said dielectric layer is thinned by a chemical mechanical polishing and an etching back processes.

7. The method according to claim 1, wherein said base layer comprises a SiGe layer.

8. A fabrication method for heterojunction bipolar transistor, said method comprising:

providing a substrate having a collector therein, a base layer over said substrate, a first emitter layer over said base layer, and a first dielectric layer over said first emitter layer;

forming a first photoresist layer over said first dielectric layer;

transferring a line pattern into said first photoresist layer by a photo mask with said line pattern to form a emitter window pattern;

etching said first dielectric layer to expose said first emitter layer by using said emitter window pattern as an etching mask;

removing said emitter window pattern;

etching said first emitter layer to expose said base layer;

forming a first oxide layer over said base layer and said first emitter layer;

forming a second oxide over said first dielectric layer and said first oxide layer;

performing a first ion implantation process into said base layer to form a first extrinsic base region therein;

forming a second dielectric layer over said second oxide layer;

anisotropically etching said second dielectric layer to expose said second oxide layer and form a spacer;

performing a second ion implantation process to form a second extrinsic base region;

forming a third dielectric layer over said second oxide layer and said spacer;

thinning said third dielectric layer to expose said second oxide layer;

removing said exposed second oxide layer and said first dielectric layer to expose said first emitter layer;

forming a second emitter layer over said first emitter layer and said third dielectric layer;

forming a second photoresist layer over said second emitter layer;

transferring an emitter pattern into said second photoresist layer;

and etching said second emitter layer, said third dielectric layer, said second oxide layer and said first oxide layer to form an emitter and

expose said second extrinsic base region.

9. The method according to claim 8, wherein said base layer comprises a SiGe layer.

10. The method according to claim 8, wherein said first dielectric layer comprises a Tetra Ethyl Ortho Silicate Glass (TEOS) layer.

11. The method according to claim 8, further comprising a step of forming a bottom anti-reflecting coating layer over said first dielectric layer.

12. The method according to claim 8, wherein said first oxide layer comprises an in situ steam generation oxide layer.

13. The method according to claim 8, wherein said second oxide layer comprises a linear oxide layer.

14. The method according to claim 8, wherein said second dielectric layer comprises a SiN layer.

15. The method according to claim 8, wherein said third dielectric layer comprises a SiN layer.

16. The method according to claim 8, wherein said third dielectric layer is thinned by a chemical mechanical polishing and an etching back processes.

CLAIMS 17-21. (CANCELLED)